CLAIMS

1. A palladium-plated lead finishing structure characterized in that Pd or a Pd alloy is plated to a thickness of not more than 0.3 μm on the surfaces of the external connection terminals of a semiconductor part using copper or a copper alloy-based material, without interposing any underlying layer or any intermediate metal layer between said material and said Pd- or Pd alloy-plated layer.

2. The palladium-plated lead finishing structure according to claim 1, wherein Au or an Au alloy is plated to a thickness of not more than 0.1 μm on the top of said Pd or Pd alloy layer.

3. A palladium-plated lead finishing structure characterized in that Pd or a Pd alloy is plated to a thickness of not more than 0.3 μm on the surfaces of the external connection terminals of a semiconductor part using iron or an iron-nickel-based material, without interposing any underlying layer or any intermediate metal layer between said material and said Pd- or Pd alloy-plated layer.

4. The palladium-plated lead finishing structure according to claim 3, wherein Au or an Au alloy is plated to a thickness of not more than 0.1 μm on the top of said Pd or Pd alloy layer.

5. A method of producing a semiconductor device characterized by plating Pd or a Pd alloy, to a thickness of not larger than 0.3 μm, on the surfaces of the external connection terminals of a semiconductor part using copper or a copper alloy-based material, without interposing any underlying layer or any intermediate metal layer between the surfaces of said material of the external connection terminals and said Pd- or Pd alloy-plated layer after at least the steps of mounting a semiconductor chip by die attachment, wire bonding and resin molding.

6. A method of producing a semiconductor device characterized by plating Pd or a Pd alloy to a thickness of not more than 0.3 μm on the surfaces of the external connection terminals of a semiconductor part using iron or an iron-nickel-based material, without interposing any underlying layer or any intermediate metal layer between the surfaces of said material of the external connection terminals and said Pd- or Pd alloy-plated layer after at least the steps of mounting a semiconductor chip by die attachment, wire bonding and resin molding.